Method of Forming a Source/Drain and a Transistor Employing the Same

TECHNICAL FIELD

[0001]   The present invention is directed, in general, to semiconductor devices and, more specifically, to a method of forming a source/drain having a reduced junction capacitance, a related method of forming a transistor, and a transistor employing the same.

BACKGROUND

[0002]   A transistor is generally formed by a self-aligned polysilicon gate process wherein a source/drain is formed adjacent to a gate by an ion implantation process using the gate as a mask. The source/drain is thereby self-aligned to a gate electrode of the gate. A channel region directly under the gate is also defined by the gate electrode. In order to reduce hot electron injection into the channel region, a source/drain dopant is implanted into a recess adjacent the gate. This lightly doped region is commonly referred to as a lightly doped drain region. The gate serves as a mask for the implant and the source/drain dopant tends to diffuse under a portion of the gate during subsequent thermal processing thereof. Thus, the lightly doped drain region is located adjacent and underlies a portion of the gate. Thereafter, spacers are formed alongside the gate electrode and another source/drain dopant is implanted to form the source/drain. The main section of the source/drain is laterally spaced away from an edge of the gate by the spacer thickness. The source/drain, therefore, consists of a main doped portion to which an external contact is made and the lightly doped drain region adjacent the channel region.

[0003]   In accordance with a trend toward higher packaging density, transistor features are becoming increasingly smaller resulting in a shorter channel region. A shorter channel region,

however, can lead to short channel effects that affect the device performance. In conventional lightly doped drain processes, short channel effects are compensated by implanting shallower junctions which come at the expense of high impurity concentrations. As a consequence, the resultant lower impurity concentrations cause undesirably high source and drain series resistance. There have been several attempts in the past to form improved shallow, lightly doped drain regions. For instance, U.S. Patent No. 6,627,502 entitled "Method for Forming High Concentration Shallow Junctions for Short Channel MOSFETs," issued September 30, 2003, to Cho, which is commonly assigned with the present invention and incorporated herein by reference, provides a lightly doped drain region by forming shallow lightly doped drain diffusions using polysilicon sidewalls as a diffusion source. Cho and many others continue to investigate processes that provide improved shallow, lightly doped drain regions.

[0004] Additionally, as the source/drain is formed in contact with a substrate, a P-N junction is formed within the transistor. At the P-N junction, holes from P-side diffuse into the N-side, while electrons from N-side diffuse into the P-side. As a consequence, an internal field is built, and an electrically neutral depletion region is formed therebetween. The depletion region plays a role as a dielectric layer between the gate and source/drain electrodes which causes a junction capacitance.

[0005] A magnitude of the junction capacitance depends on a width of the depletion regions, and the width of depletion regions is related to a junction profile of the implanted ions in the substrate. Because of an abrupt junction profile of arsenic ions, for instance, the width of the depletion region is narrow, and the junction capacitance may become large. Additionally, the high energy implanted arsenic ions create defects in the silicon crystal structure of the substrate, which can lead to leakage in the source/drain.

[0006]   Analogous to the continuous efforts to develop new processes for the lightly doped drain regions, there have been attempts in the past to reduce junction capacitance associated with the gate and source/drain electrodes of the transistor. For instance, U.S. Patent No. 6,274,448 entitled "Method of suppressing junction capacitance of source/drain regions," issued August 14, 2001 to Lin, *et al.*, which is incorporated by reference, discloses a method of suppressing junction capacitance associated with a transistor. The source/drains are formed by double implantation of phosphorus ions and arsenic ions. The phosphorus ion implantation lowers an energy needed in the implantation of arsenic ions and reduces dislocations in the source/drains formed during the implantation of the arsenic ions. Further, the double implantation suppresses a junction profile of the arsenic ions and enhances the width of depletion regions. As a result, the junction capacitance is reduced, thereby accelerating a function of the transistor. (Abstract of Lin, *et al.*). While Lin, *et al.* provides a solution to lowering a junction capacitance associated with a transistor, there is still a need in the art to provide other processes and structures that reduce a junction capacitance thereof.

[0007]   Accordingly, what is needed in the art is a transistor and related process of forming the transistor that overcomes short channel effects while at the same time reducing a junction capacitance thereof that improves upon or resolves the deficiencies in the prior art.

SUMMARY OF THE INVENTION

[0008]   These and other problems are generally solved or circumvented, and technical advantages are generally achieved, by advantageous embodiments of the present invention which includes a method of forming a source/drain and a transistor employing the same. In one embodiment, the method of forming the source/drain includes forming a recess in a substrate adjacent a gate of the transistor and forming a deep doped region below a bottom surface of the recess. The method also includes epitaxially growing a semiconductor material within the recess and forming a lightly doped drain region adjacent the gate.

[0009]   In another aspect, the present invention provides a transistor and a method of forming the transistor. In one embodiment, the transistor includes a gate formed on a substrate having a gate dielectric and a gate electrode formed thereon. The transistor also includes a source and a drain, each formed in a recess of the substrate adjacent opposite sides of the gate. The source and drain each include a lightly doped drain region adjacent the gate and a deep doped region below a bottom surface of the recess.

[0010]   The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention. It should be appreciated by those skilled in the art that the conception and specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures or processes for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that

such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011]   For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0012]   FIGUREs 1 to 13 illustrate cross sectional views of an embodiment of constructing a transistor according to the principles of the present invention; and

[0013]   FIGUREs 14 to 25 illustrate cross sectional views of another embodiment of constructing a transistor according to the principles of the present invention.

[0014]   Corresponding numerals and symbols in the different figures generally refer to corresponding parts unless otherwise indicated. The figures are drawn to clearly illustrate the relevant aspects of the preferred embodiments and are not necessarily drawn to scale.

DETAILED DESCRIPTION OF ILLUSTRATIVE EMBODIMENTS

[0015]   The making and using of the presently preferred embodiments are discussed in detail below. It should be appreciated, however, that the present invention provides many applicable inventive concepts that can be embodied in a wide variety of specific contexts. The specific embodiments discussed are merely illustrative of specific ways to make and use the invention, and do not limit the scope of the invention.

[0016]   The present invention will be described with respect to preferred embodiments in a specific context, namely, a method of forming a transistor and a transistor employing the same.

The principles of the present invention, however, may also be applied to other semiconductor devices of like construction. The advantages associated with the method and resulting transistor further exploit the benefits associated with the application of low junction transistors in electronic devices.

[0017] Referring to FIGUREs 1-13, illustrated are cross sectional views of an embodiment of constructing a transistor according to the principles of the present invention. Beginning with FIGURE 1, a gate 105 is formed over a substrate 110 (e.g., composed of silicon or silicon-germanium) employing conventional semiconductor processes. The substrate 110 may be a semiconductor layer formed over a buried oxide layer using silicon-on-insulator technology. In the present embodiment, a process of constructing a first transistor 115 (e.g., a P-type metal oxide semiconductor) and a second transistor 120 (e.g., a N-type metal oxide semiconductor) are illustrated and described. Of course, the processes described herein are equally applicable to other types of transistors as well. In the interim processing step illustrated in FIGURE 1, the first transistor 115 includes a gate 105 having a gate dielectric 125, a gate electrode 130, and a hard mask 135 on a top surface thereof. Similarly, the second transistor 120 includes a gate 105 having a gate dielectric 125, a gate electrode 130, and a hard mask 135 on a top surface thereof.

[0018] In the illustrated embodiment, the first and second transistors 115, 120 are self-aligned transistors and are shown at a point in the process wherein the gates 105 have been patterned by, for instance, anisotropic dry etching. The dry etching may be either reactive ion etching or plasma etching, which are well known and widely accepted practices by those skilled in the art. The substrate 110 includes shallow trench isolation regions 140 formed by conventional processes. Those skilled in the art understand that isolation regions may be formed using conventional methods such as a local oxidation of silicon process.

[0019]   As mentioned above, the gates 105 of the first and second transistors 115, 120 include the gate dielectric 125 which may be composed of a gate oxide layer (*e.g.*, a thermally grown oxide or nitrided oxide) or a layer of high "k" dielectric material. While the gate electrode 130 of the first and second transistors 115, 120 is composed of a polysilicon layer, those skilled in the art recognize that other materials such as metals (*e.g.*, tungsten, tantalum, aluminum, nickel, ruthenium, rhodium, palladium, platinum, titanium, or molybdenum) and metal compounds (*e.g.*, titanium nitride and tantalum nitride) may also be employed to advantage. The hard mask 135 of the first and second transistors 115, 120 is typically formed from a silicon oxide cap, a silicon nitride cap or a combination thereof.

[0020]   The layers that form the gate electrode 130 and hard mask 135 are typically blanket deposited by a chemical vapor deposition process. The processes for forming the gates 105 of the first and second transistors 115, 120 are well known to those skilled in the art. In an exemplary embodiment, the gate dielectric 125 may be about 0.5 to 8 nanometers (nm) thick and the gate electrode 130 may be about 50 to 150 nm thick. The gate electrode 130 may consist of a single uniformly doped polysilicon layer or it may have an upper heavily doped portion and a lower undoped portion. The hard mask 135 may be about 10 to 100 nm thick.

[0021]   Turning now to FIGURE 2, the first and second transistors 115, 120 are placed in an oxidizing environment and exposed regions of silicon including the substrate 110 and polysilicon layers of the gates 105 are oxidized or deposited to form an oxide layer 145 about the first and second transistors 115, 120. The shallow trench regions 140 and the hard mask 135 (if formed by an oxide material) may also have an oxide layer formed on exposed surfaces thereof. For purposes of clarity, however, an oxide layer is not illustrated on the shallow trench regions 140 and the hard mask 135 of the first and second transistors 115, 120.

[0022]   Turning now to FIGUREs 3 and 4, an insulating layer 150 (*e.g.*, a silicon nitride, silicon oxide or a combination thereof) is blanket deposited over the substrate 110 and first and second transistors 115, 120 using, for instance, a chemical vapor deposition or a plasma enhanced chemical vapor deposition. Thereafter, temporary spacers 155 are formed about the gates 105 of the first and second transistors 115, 120 by plasma dry etching the insulating layer until the planar portions of the substrate 110 and hard mask 135 of the gates 105 of the first and second transistors 115, 120 are reached. As depicted in FIGURE 4, the temporary spacers 155 are highly tapered toward the hard mask 135 of the gates 105 of the first and second transistors 115, 120 and, typically, range from 5 to 100 nm wide.

[0023]   Turning now to FIGURE 5, lateral recesses (hereinafter referred to as "recesses") 160 in which will be formed a source 165 and drain 170 of the first and second transistors 115, 120 are formed by etching the substrate 110 adjacent the gates 105 thereof. The recesses 160 are self-aligned with the temporary spacers 155 about the gates 105 of the first and second transistors 115, 120. As well understood by those skilled in the art, etching the substrate 110 may be accomplished by many processes such as a chemical dry etching process.

[0024]   The dimensions and depth of the recesses 160 are a function of the desired features and characteristics of the first and second transistors 115, 120. As an example, if one of the first and second transistors 115, 120 is a logic device, then a gate length may equal 5 to 20nm, 20 to 40 nm, and 40 to 60 nm, depending on a technology node employed, and a depth of the recesses 160 may be in the range of 5 to 20 nm, 20 to 50 nm and 50 to 100 nm, depending on a technology node employed and, preferably, a depth of 20 to 50 nm, for a 65 nm technology node. Although the recesses 160 for the source 165 and drain 170 of the first and second transistors 115, 120 are illustrated as symmetrical, those skilled in the art recognize that the recess 160 for

the source 165 may have different dimensions (*e.g.*, be shallower or deeper) than the recess 160 for the drain 170 and vice versa.

[0025]   Turning now to FIGURE 6, a region of the first transistor 115 is protected by a photo resist layer 175 and an ion implantation process is performed to form a deep doped region 180 below a bottom surface of the recesses 160 for the source 165 and drain 170 of the second transistor 120. Typically, to form the deep doped regions 180 in the second transistor 120 (a N-type metal oxide semiconductor), arsenic ions are implanted into the substrate 110 and the gate 105 and temporary spacers 155 serve as a mask. Of course, other N-type dopants such as antimony and phosphorous may also be employed to form the deep doped region 180. The ion implantation process of arsenic may be performed at an energy level of about 5 to 15 keV and at a dose of 5×10^{12} to 1×10^{14} atoms/cm^2. The photo resist layer 175 that protects a region of the first transistor 115 is thereafter removed by, for instance, ashing or the like as well understood by those skilled in the art.

[0026]   Turning now to FIGURE 7, a region of the second transistor 120 is then protected by a photo resist layer 175 and an ion implantation process is performed to form a deep doped region 180 below a bottom surface of the recesses 160 for the source 165 and drain 170 of the first transistor 115. Typically, to form the deep doped regions 180 in the first transistor 115 (a P-type metal oxide semiconductor), boron ions are implanted into the substrate 110 and the gate 105 and temporary spacers 155 serve as a mask. Of course, other P-type dopants such as boron difluoride may also be employed to form the deep doped region 180. The ion implantation process of boron may be performed at an energy level of about 0.5 to 10 keV and at a dose of 5 $\times 10^{12}$ to 1×10^{14} atoms/cm^2. Again, the photo resist layer 175 that protects the region of the

second transistor 120 is thereafter removed by, for instance, ashing or the like as well understood by those skilled in the art.

[0027] Turning now to FIGURE 8, a selective epitaxial growth process such as a molecular beam epitaxial growth process is performed to deposit, for instance, silicon, silicon germanium or silicon carbon at a thickness of 30 to 50 nm, 50 to 100 nm, or 100 to 150 nm within the recesses 160 for the source 165 and drain 170 of the first and second transistors 115, 120. Alternatively, the source 165 and drain 170 of the first and second transistors 115, 120 may be formed by performing a selective ultra high vacuum chemical vapor deposition or atomic layer deposition of the silicon, silicon germanium or silicon carbon. Thereafter, the temporary spacers 155 and the hard mask 135 about the gates 105 of the first and second transistors 115, 120 are removed.

[0028] Turning now to FIGURE 9, the region of the first transistor 115 is then protected by a photo resist layer 175 and an ion implantation process is performed to form a lightly doped drain region 185 adjacent and slightly under the gate 105 of the second transistor 120. Typically, to form the lightly doped drain regions 185 of the second transistor 120 (a N-type metal oxide semiconductor), arsenic ions are implanted into the substrate 110 and the gate 105 serves as a mask. Of course, other N-type dopants such as antimony and phosphorous may also be employed to form the lightly doped drain regions 185 for the second transistor 120. The ion implantation process of arsenic may be performed at an energy level of about 0.5 to 5 keV and at a dose of 5×10^{14} to 2×10^{15} atoms/cm^2.

[0029] Since the temporary spacers 155 about the gate 105 of the second transistor 120 have been removed, the lightly doped drain regions 185 thereof are not spaced apart from, but in fact align with, the edges of the gate 105. In fact, the lightly doped drain regions 185 underlie a

portion of the gate 105 of the second transistor 120. As clearly understood by those skilled in the art, the arsenic ions diffuse under the gate 105 during subsequent thermal processing. The out-diffusion, as it is referred to, is desirable to achieve a shorter effective channel length under the gate 105 of the second transistor 120. Again, the photo resist layer 175 that protects region of the first transistor 115 is thereafter removed by, for instance, ashing or the like as well understood by those skilled in the art.

[0030] Turning now to FIGURE 10, the region of the second transistor 120 is then protected by a photo resist layer 175 and an ion implantation process is performed to form a lightly doped drain region 185 adjacent and slightly under the gate 105 of the first transistor 115. Typically, to form the lightly doped drain regions 185 of the first transistor 115 (a P-type metal oxide semiconductor), boron ions are implanted into the substrate 110 and the gate 105 serves as a mask. Of course, other P-type dopants such as boron difluoride may also be employed to form the lightly doped drain regions 185 for the first transistor 115. The ion implantation process of boron may be performed at an energy level of about 0.5 to 5 keV and at a dose of 5×10^{14} to 2×10^{15} atoms/cm^2.

[0031] Analogous to discussion above, since the temporary spacers 155 about the gate 105 of the first transistor 115 have been removed, the lightly doped drain regions 185 thereof are not spaced apart from, but in fact align with, the edges of the gate 105. In fact, the lightly doped drain regions 185 underlie a portion of the gate 105 of the first transistor 115. As clearly understood by those skilled in the art, the boron ions diffuse under the gate 105 during subsequent thermal processing. The out-diffusion is desirable to achieve a shorter effective channel length under the gate 105 of the first transistor 115. Again, the photo resist layer 175

that protects the region of the second transistor 120 is thereafter removed by, for instance, ashing or the like as well understood by those skilled in the art.

[0032] Turning now to FIGURE 11, analogous to constructing the temporary spacers 155 as described above, an insulating layer (*e.g.*, a silicon nitride, silicon oxide or a combination thereof) is blanket deposited over the substrate 110 and first and second transistors 115, 120. Thereafter, spacers 190 are formed about the gates 105 of the first and second transistors 115, 120 by plasma dry etching the insulating layer until the planar portions of the substrate 110 and a top surface of the gate 105 of the first and second transistors 115, 120 are reached. As depicted in FIGURE 11, the spacers 190 are highly tapered toward a top surface of the gate electrodes 130 of the first and second transistors 115, 120 and, typically, range from 10 to 20 nm, 20 to 40 nm, 40 to 60 nm, or 60 to 100 nm wide, depending on a technology node employed.

[0033] The region of the first transistor 115 is then protected by a photo resist layer 175 and an ion implantation process is performed to dope the epitaxial grown source 165 and drain 170 of the second transistor 120. Typically, to dope the source 165 and drain 170 of the second transistor 120 (a N-type metal oxide semiconductor), arsenic ions are implanted into the substrate 110 and the gate 105 and spacers 190 serve as a mask. Of course, other N-type dopants such as antimony and phosphorous may also be introduced to dope the source 165 and drain 170 of the second transistor 120. The ion implantation process of arsenic may be performed at an energy level of about 10 to 30 keV and at a dose of 5×10^{12} to 5×10^{15} atoms/cm^2. While an ion implantation process has been described to dope the epitaxial gown source 165 and drain 170, those skilled in the art will recognize that other processes such as an *in situ* doped epitaxial growth process may be employed to introduce N-type dopants into the source 165 and drain 170 of the second transistor 120 during the epitaxial growth process. Again, the photo resist layer

175 that protects the region of the first transistor 115 is thereafter removed by, for instance, ashing or the like as well understood by those skilled in the art.

[0034]   Turning now to FIGURE 12, the region of the second transistor 120 is then protected by a photo resist layer 175 and an ion implantation process is performed to dope the epitaxial grown source 165 and drain 170 of the first transistor 115. Typically, to dope the source 165 and drain 170 of the first transistor 115 (a P-type metal oxide semiconductor), boron ions are implanted into the substrate 110 and the gate 105 and spacers 190 serve as a mask. Of course, other P-type dopants such as boron difluoride may also be introduced to dope the source 165 and drain 170 of the first transistor 115. The ion implantation process of boron may be performed at an energy level of about 1 to 20 keV and at a dose of 5×10^{12} to 5×10^{15} atoms/cm^2. Again, while an ion implantation process has been described to dope the epitaxial gown source 165 and drain 170, those skilled in the art will recognize that other processes such as an *in situ* doped epitaxial growth process may be employed to introduce P-type dopants into the source 165 and drain 170 of the first transistor 115 during the epitaxial growth process. Again, the photo resist layer 175 that protects the region of the second transistor 120 is thereafter removed by, for instance, ashing or the like as well understood by those skilled in the art.

[0035]   Turning now to FIGURE 13, a salicide process is hereinafter performed to create enhanced contacts 195 for the gate 105, source 165 and drain 170 of the first and second transistors 115, 120. The salicide processing involves deposition of a metal that forms an intermetallic compound with silicon, but does not react with silicon oxides, nitrides, or oxynitrides under normal processing conditions. Metals commonly employed in salicide processing include platinum, titanium, nickel, tungsten and cobalt, each of which forms very low resistivity phases with silicon. The metal is deposited in a substantially uniform thickness over

all exposed surface features of the substrate 110 and the first and second transistors 115, 120, preferably by a physical vapor deposition process (*e.g.*, sputtering from an ultra pure target utilizing an ultra-high vacuum, multi-chamber DC magnetron sputtering system).

[0036]   After deposition, the metal layer blankets a top surface of the gate electrode 130, the spacers 190 about the gate 105, the doped regions of the source 165 and drain 170, and the shallow trench isolation regions 140. As a result of thermal processing (*e.g.*, a rapid thermal annealing process), the metal layer reacts with underlying silicon to form electrically conductive metal silicide layers on a top surface of the gate 105, source 165 and drain 170 of the first and second transistors 115, 120. Unreacted portions of the metal layer (*e.g.*, the spacers 190 about the gate 105 and the shallow trench isolation regions 140) are then removed employing, for instance, a wet chemical etching process selective to the metal silicide layers. The metal silicide layers form enhanced contacts 195 for the gate 105, source 165 and drain 170 of the first and second transistors 115, 120.

[0037]   Thus, the aforementioned processes provide first and second transistors 115, 120 with enhanced characteristics. For instance, an implant energy of deep doped region 180 is pretty low so that the dopants will not implant through the gate electrode 130 and will not damage the gate dielectric 125. Also, a lateral diffusion of deep doped region 180 will not impact a channel region 197 underlying the gate 105 so that short channel effect can be well controlled by the lightly doped drain regions 185.

[0038]   Additionally, the first and second transistors 115, 120 exhibit a reduced junction capacitance in accordance with forming the source 165 and drain 170 over multiple processes and, especially, in view of the deep doped regions 180 thereof. For instance, the reduced junction capacitance is a function of the graded characteristic of the source 165 and drain 170 in

accordance with the lightly doped drain regions 185 through the deep doped regions 180. Looking at the first transistor 115 (a P-type metal oxide semiconductor) as an example, the multiple boron ion implants associated with the first transistor 115 suppress a junction profile of the doped ions in the substrate 110. Consequently, a junction capacitance of the first transistor 115 is reduced and an operational switching period thereof can be upgraded. Of course, an analogous benefit is achieved via the construction of and provided by the second transistor 120 as well.

[0039]   Turning now to FIGUREs 14-25, illustrated are cross sectional views of another embodiment of constructing a transistor according to the principles of the present invention. Inasmuch as many of the processes to construct and characteristics of the transistors illustrated in FIGUREs 14-25 are analogous to the processes to construct and characteristics of the transistors described with respect to FIGUREs 1-13, many of the details regarding the construction thereof will hereinafter be omitted. It is contemplated that higher temperatures (*e.g.*, equal to or greater than 650 degrees Celsius) are employed for the selective epitaxial growth process for the transistors described with respect to FIGUREs 1-13. An advantage of using the lower temperatures is that dopant diffusion caused from thermal processes may be avoided. Conversely, the processes to construct the transistors illustrated in FIGUREs 14-25 generally employ lower temperatures (*e.g.*, 300 to 650 degrees Celsius) for the selective epitaxial growth process.

[0040]   Beginning with FIGURE 14, a gate 205 (*e.g.*, a polysilicon gate) is formed over a substrate 210 (*e.g.*, a silicon substrate) employing conventional semiconductor processes. In the present embodiment, a process of constructing a first transistor 215 (*e.g.*, a P-type metal oxide semiconductor) and a second transistor 220 (*e.g.*, a N-type metal oxide semiconductor) are

illustrated and described. In the interim processing step illustrated in FIGURE 14, the first transistor 215 includes a gate 205 having a gate dielectric 225, a gate electrode 230, and a hard mask 235 on a top surface thereof. Similarly, the second transistor 220 includes a gate 205 having a gate dielectric 225, a gate electrode 230, and a hard mask 235 on a top surface thereof. The substrate 210 includes shallow trench isolation regions 240 formed by conventional methods.

[0041]   Turning now to FIGURE 15, the first and second transistors 215, 220 are placed in an oxidizing environment and exposed regions of silicon including the substrate 210 and polysilicon layers of the gates 205 are oxidized or deposited to form an oxide layer 245 about the first and second transistors 215, 220. The shallow trench regions 240 and the hard mask 235 (if formed by an oxide material) may also have an oxide layer formed on exposed surfaces thereof. For purposes of clarity, however, an oxide layer is not illustrated on the shallow trench regions 240 and the hard mask 235 of the first and second transistors 215, 220.

[0042]   A region of the first transistor 215 is then protected by a photo resist layer 250 and an ion implantation process is performed to form a lightly doped drain region 255 adjacent and slightly under the gate 205 of the second transistor 220. Typically, to form the lightly doped drain regions 255 of the second transistor 220 (a N-type metal oxide semiconductor), arsenic ions are implanted into the substrate 210 and the gate 205 serves as a mask. As illustrated, the lightly doped drain regions 255 are not spaced apart from, but in fact align with, the edges of the gate 205. In fact, the lightly doped drain regions 255 underlie a portion of the gate 205, which provides a shorter effective channel length under the gate 205 of the second transistor 220. The photo resist layer 250 that protects the region of the first transistor 215 is thereafter removed as well understood by those skilled in the art.

[0043] Turning now to FIGURE 16, a region of the second transistor 220 is then protected by a photo resist layer 250 and an ion implantation process is performed to form a lightly doped drain region 255 adjacent and slightly under the gate 205 of the first transistor 215. Typically, to form the lightly doped drain regions 255 of the first transistor 215 (a P-type metal oxide semiconductor), boron ions are implanted into the substrate 210 and the gate 205 serves as a mask. Analogous to discussion above, the lightly doped drain regions 255 underlie a portion of the gate 205 of the first transistor 215, which provides a shorter effective channel length under the gate 205 of the first transistor 215. Again, the photo resist layer 250 that protects the region of the second transistor 220 is thereafter removed as well understood by those skilled in the art.

[0044] Turning now to FIGUREs 17 and 18, an insulating layer 260 (*e.g.*, a silicon nitride, silicon oxide or a combination thereof) is blanket deposited over the substrate 210 and first and second transistors 215, 220 using, for instance, a chemical vapor deposition or a plasma enhanced chemical vapor deposition. Thereafter, spacers 265 are formed about the gates 205 of the first and second transistors 215, 220 by plasma dry etching the insulating layer until the planar portions of the substrate 210 and hard mask 235 of the gates 205 of the first and second transistors 215, 220 are reached (see FIGURE 18).

[0045] Turning now to FIGURE 19, recesses 270 in which will be formed a source 275 and drain 280 of the first and second transistors 215, 220 are formed by etching the substrate 210 adjacent the gates 205 thereof. The recesses 270 are self aligned with the spacers 265 about the gates 205 of the first and second transistors 215, 220. As illustrated, the lightly doped drain regions 255 underlying the spacers 265 about the gates 205 of the first and second transistors 215, 220 are not etched away and remain intact.

[0046]   Turning now to FIGURE 20, the region of the first transistor 215 is protected by a photo resist layer 250 and an ion implantation process is performed to form a deep doped region 285 below a bottom surface of the recesses 270 for the source 275 and drain 280 of the second transistor 220. Typically, to form the deep doped regions 285 in the second transistor 220 (a N-type metal oxide semiconductor), arsenic ions are implanted into the substrate 210 and the gate 205 and spacers 265 serve as a mask. Again, the photo resist layer 250 that protects the region of the first transistor 215 is thereafter removed as well understood by those skilled in the art.

[0047]   Turning now to FIGURE 21, the region of the second transistor 220 is then protected by a photo resist layer 250 and an ion implantation process is performed to form a deep doped region 285 below a bottom surface of the recesses 270 for the source 275 and drain 280 of the first transistor 215. Typically, to form the deep doped regions 285 in the first transistor 215 (a P-type metal oxide semiconductor), boron ions are implanted into the substrate 210 and the gate 205 and spacers 265 serve as a mask. Again, the photo resist layer 250 that protects region of the second transistor 220 is thereafter removed as well understood by those skilled in the art.

[0048]   Turning now to FIGURE 22, a selective epitaxial growth process is performed to deposit, for instance, silicon, silicon germanium or silicon carbon within the recesses 270 for the source 275 and drain 280 of the first and second transistors 215, 220. Thereafter, the hard mask 235 about the gates 205 of the first and second transistors 215, 220 are removed.

[0049]   Turning now to FIGURE 23, the region of the first transistor 215 is then protected by a photo resist layer 250 and an ion implantation process is performed to dope the epitaxial grown source 275 and drain 280 of the second transistor 220. Typically, to dope the source 275 and drain 280 of the second transistor 220 (a N-type metal oxide semiconductor), arsenic ions are implanted into the substrate 210 and the gate 205 and spacers 265 serve as a mask. Again, the

photo resist layer 250 that protects the region of the first transistor 215 is thereafter removed as well understood by those skilled in the art.

[0050] Turning now to FIGURE 24, the region of the second transistor 220 is then protected by a photo resist layer 250 and an ion implantation process is performed to dope the epitaxial grown source 275 and drain 280 of the first transistor 215. Typically, to dope the source 275 and drain 280 of the first transistor 215 (a P-type metal oxide semiconductor), boron ions are implanted into the substrate 210 and the gate 205 and spacers 265 serve as a mask. Again, the photo resist layer 250 that protects the region of the second transistor 220 is thereafter as well understood by those skilled in the art.

[0051] Turning now to FIGURE 25, a salicide process is hereinafter performed to create enhanced contacts 290 for the gate 205, source 275 and drain 280 of the first and second transistors 215, 220. A metal is deposited in a substantially uniform thickness over all exposed surface features of the substrate 210 and the first and second transistors 215, 220. As a result of thermal processing, the metal layer reacts with underlying silicon to form electrically conductive metal silicide layers on a top surface of the gate 205, source 275 and drain 280 of the first and second transistors 215, 220. Unreacted portions of the metal layer (*e.g.*, the spacers 265 about the gate 205 and the shallow trench isolation regions 240) are then removed. The metal silicide layers form enhanced contacts 290 for the gate 205, source 275 and drain 280 of the first and second transistors 215, 220. As mentioned above, the first and second transistors 215, 220 exhibit a reduced junction capacitance in accordance with forming the source and drain 275, 280 over multiple processes and, especially, in view of the deep doped regions 285 thereof.

[0052] Thus, a method of forming a source/drain, a method of forming a transistor and a transistor with readily attainable and quantifiable advantages has been introduced. Those skilled

in the art should understand that the previously described embodiments of the transistor and related method of forming the transistor are submitted for illustrative purposes only and that other embodiments capable of providing a deep doped region in a semiconductor device are well within the broad scope of the present invention.

[0053]   Also, although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims. For example, many of the processes discussed above can be implemented in different methodologies and replaced by other processes, or a combination thereof.

[0054]   Moreover, the scope of the present application is not intended to be limited to the particular embodiments of the process, machine, manufacture, composition of matter, means, methods and steps described in the specification. As one of ordinary skill in the art will readily appreciate from the disclosure of the present invention, processes, machines, manufacture, compositions of matter, means, methods, or steps, presently existing or later to be developed, that perform substantially the same function or achieve substantially the same result as the corresponding embodiments described herein may be utilized according to the present invention. Accordingly, the appended claims are intended to include within their scope such processes, machines, manufacture, compositions of matter, means, methods, or steps.